This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (currently amended) A semiconductor device comprising:

an integrated circuit chip having an outline, active and passive surfaces, and active components including a plurality of contact pads, spaced apart by less than 100 μm center to center, on said active surface;

a plurality of electrical coupling members attached to said contact pads, said coupling members selected from a group consisting of gold bumps, copper bumps, copper/nickel/palladium bumps, and z-axis conductive epoxy;

an electrically insulating thin-film interposer having first and second surfaces and wherein the thin-film interposer is made of insulating materials such as polyimide, Kapton, Upilex, PCB resin, FR-4 and cyanate ester resin, and the thin-film is in the thickness range of about 40 to 80 um, a plurality of electrically conductive lines integral with said first surface, a plurality of electrically conductive paths extending through said interposer, contacting said conductive lines and forming exit ports on said second surface;

said chip coupling members attached to said conductive lines, covering an area portion of said first interposer surface; and

encapsulation material protecting said passive chip surface and at least a portion of said first interposer surface not covered by said attached chip.

2. (original) The device according to Claim 1 further having solder balls attached to said exit ports on said second interposer surface.

3. (original) The device according to Claim 1 further having an adhesive non-conductive polymer underfilling any spaces between said chip coupling members attached to said conductive lines under said chip.

4. (original) The device according to Claim 1 wherein said interposer is a polyimide film.

5. (original) The device according to Claim 1 wherein said interposer has an outline larger than said outline of said chip.

6. (original) The device according to Claim 1 wherein said electrically conductive lines are made of a material selected from a group consisting of copper, copper alloy, or copper plated with tin, tin alloy, silver, or gold.

7. (previously presented) The device according to Claim 1 wherein said coupling member attachment is provided by metal interdiffusion of thermo-compression bonding.

8. (original) The device according to Claim 1 wherein said encapsulation material is a molding compound.

9. (previously presented) The device according to Claim 9 wherein said molding compound has the same outline as said interposer.

10. (currently amended) A semiconductor device comprising:

an integrated circuit chip having an outline, active and passive surfaces, and active components including a plurality of contact pads on said active surface;

a plurality of electrical coupling members attached to said contact pads, said coupling members selected from a group consisting of gold bumps, copper bumps, copper/nickel/palladium bumps, and z-axis conductive epoxy;

an electrically insulating thin-film interposer having first and second surfaces<u>and wherein the thin-film interposer is made of insulating materials such as polyimide, Kapton, Upilex, PCB resin, FR-4 and cyanate ester resin, and the thin-film is in the thickness range of about 40 to 80 um</u>, a plurality of electrically conductive lines integral with said first surface, a plurality of electrically conductive paths extending through said interposer, contacting said conductive lines and forming exit ports on said second surface;

said chip coupling members attached to said conductive lines, covering an area portion of said first interposer surface; and

encapsulation material protecting said passive chip surface and at least a portion of said first interposer surface not covered by said attached chip.

11-16 (canceled)

17. (currently presented) A semiconductor device comprising:

an integrated circuit chip having an outline, active and passive surfaces, and active components including a plurality of contact pads on said active surface;

a plurality of electrical coupling members attached to said contact pads;

an electrically insulating thin-film interposer having first and second surfaces and wherein the thin-film interposer is made of insulating materials such as polyimide, Kapton, Upilex, PCB resin, FR-4 and cyanate ester resin, and the thin-film is in the thickness range of about 40 to 80 um, a plurality of electrically conductive lines integral with said first surface, a plurality of electrically conductive paths extending through said interposer, contacting said conductive lines and forming exit ports on said second surface;

said chip coupling members interdiffused with said conductive lines; and

encapsulation material protecting said passive chip surface and at least a portion of said first interposer surface not covered by said attached chip.

18. (previously presented) The device according to Claim 17 further having solder balls attached to said exit ports on said second interposer surface.

19. (previously presented) The device according to Claim 17 further having an adhesive non-conductive polymer underfilling any spaces between said chip coupling members attached to said conductive lines under said chip.

20. (previously presented) The device according to Claim 17 wherein said interposer is a polyimide film.

21. (previously presented) The device according to Claim 17 wherein said interposer has an outline larger than said outline of said chip.

22. (previously presented) The device according to Claim 17 wherein said electrically conductive lines are made of a material selected from a group consisting of copper, copper alloy, or copper plated with tin, tin alloy, silver, or gold.

23. (previously presented) The device according to Claim 17 wherein said encapsulation material is a molding compound.

24. (previously presented) The device according to Claim 23 wherein said molding compound has the same outline as said interposer.